

CLAIMS

What is claimed is:

- 5        1.    A method comprising:  
         receiving a plurality of frames;  
         storing the frames in a receive buffer, wherein the  
                 receive buffer is configured to be accessed in a  
                 first-in-first-out fashion;  
10        storing header information corresponding to each of the  
         frames in a header storage, wherein the header  
         storage is configured to provide access to the  
         header information in the same order as the frames;  
         retrieving header information from the header storage,  
15        wherein the header information corresponds to a  
         first frame;  
         making a routing decision for the first frame based upon  
         the header information;  
         retrieving the first frame from the receive buffer; and  
20        routing the first frame based upon the routing decision.
2.    The method of claim 1 wherein the routing decision for  
the first frame is made while a preceding frame is being  
routed.
- 25        3.    The method of claim 1 wherein routing the first frame  
comprises transmitting the first frame to the transmit buffer  
of a destination determined by the routing decision.
- 30        4.    The method of claim 1 further comprising maintaining a  
timer corresponding to each header in the header storage.

5. The method of claim 4 further comprising retrieving a timer corresponding to the retrieved header information, determining whether the timer corresponding to the retrieved header information exceeds a predetermined maximum value, and discarding the frame corresponding to the header information if the timer corresponding to the retrieved header information exceeds the predetermined maximum value.

6. The method of claim 1, further comprising snooping on received frames to identify the header information corresponding to each of the frames.

7. The method of claim 1 wherein the receive buffer is a first-in-first-out (FIFO) buffer having a head position and a tail position, wherein entries are written to the tail position and are promoted through the FIFO buffer to the head position, and wherein retrieving the first frame from the receive buffer comprises reading the frame at the head position.

8. The method of claim 7 further comprising providing a bypass circuit coupled to the header storage, wherein if no header information is available at the head of the header storage, the bypass circuit makes next-received header information immediately available.

9. A frame buffer system comprising:

a receive buffer configured to store a plurality of  
received frames, wherein the receive buffer is  
configured to be accessed in first-in-first-out  
fashion;

a header storage configured to store header information  
corresponding to each of the frames in the receive  
buffer;

transfer logic coupled to the receive buffer and header  
storage, wherein the transfer logic is configured to  
make a routing decision for each of the frames in  
the receive buffer based on the corresponding header  
information in the header storage and to transmit  
each of the frames to a destination port according  
to the corresponding routing decision.

10. The frame buffer system of claim 9 further comprising a  
snooping circuit coupled to the header storage, wherein the  
snooping circuit is configured to identify header information  
in the received frames and copy the corresponding header  
information to the header storage.

11. The frame buffer system of claim 9 further comprising a  
bypass circuit configured to receive first header information,  
wherein when header information is received, if no preceding  
header information is currently stored in the header storage,  
the bypass circuit is configured to make the first header  
information available to the transfer logic.

12. The frame buffer system of claim 9 wherein the header storage is a first-in-first-out (FIFO) buffer having a head position and a tail position, wherein header information entries are written to the tail position and are promoted through the FIFO buffer to the head position, and wherein the header information at the head position of the FIFO buffer is available to the transfer logic.

13. The frame buffer system of claim 9 wherein the header storage is a random access memory which is accessed via a head pointer which indicates a head position and a tail pointer which indicates a tail position, wherein header information is written to the tail position and are retrieved from the head position, and wherein the head and tail pointers are manipulated to promote header information in the header storage from the tail position to the head position, thereby providing circular, first-in-first-out operation of the random access memory.

14. The frame buffer system of claim 9 wherein the receive buffer is a random access memory which is accessed via a head pointer which indicates a head position and a tail pointer which indicates a tail position, wherein frames are written to the tail position and are retrieved from the head position, and wherein the head and tail pointers are manipulated to promote frames in the receive buffer from the tail position to the head position, thereby providing circular, first-in-first-out operation of the random access memory.

15. The frame buffer system of claim 9 further comprising a plurality of timers associated with the each frame in the receive buffer, wherein each timer indicates the amount of time the corresponding frame has been in the receive buffer.

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16. The frame buffer system of claim 15 wherein the timers are stored in a first-in-first-out (FIFO) timer storage, wherein the timers are promoted through the FIFO timer storage as the corresponding frames are promoted through the receive buffer.

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17. The frame buffer system of claim 15 wherein the timers are stored in a random access timer storage, wherein each timer is associated with one of the frames in the receive buffer.

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18. The frame buffer system of claim 9 further comprising a transmit timers associated with the transmit buffer, wherein the transmit timer indicates the amount of time the frame currently residing in the transmit buffer has been in the transmit buffer.

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19. A switch comprising:

a plurality of ports,

wherein at least one of the plurality of ports is  
configured to receive frames for routing to  
others of the plurality of ports

wherein the at least one port includes

a receive buffer configured to store a  
plurality of frames,

a header buffer configured to store header  
information corresponding to the frames  
stored in the receive buffer,

transfer logic coupled to the receive buffer  
and the header buffer, wherein the  
transfer logic is configured to receive  
first header information from the header  
buffer and to make a routing decision  
based upon the received header information  
for a frame in the receive buffer  
corresponding to the header information.

20. The switch of claim 19 further comprising a dedicated  
register coupled to the header buffer and the transmit logic,  
wherein the dedicated register is configured to store the  
first header information and wherein the transfer logic is  
configured to read the first header information from the  
dedicated register.

21. The switch of claim 19 wherein the first header  
information corresponds to a first frame in the receive buffer  
and wherein the transfer logic is configured to make the  
routing decision for the first frame prior to the first frame  
reaching a head position in the receive buffer.

22. The switch of claim 19 wherein the first header  
information corresponds to a first frame in the receive buffer  
and wherein the transmit logic is configured to make the  
routing decision for the first frame while a preceding frame  
is being transferred from the receive buffer.

23. The switch of claim 19 wherein the one of the ports to  
which the one of the frames is transferred comprises  
a transmit buffer,  
a header register and  
transmit logic,  
wherein the transmit buffer is configured to receive the  
one of the frames from the receive buffer and to  
store the one of the frames for transmission to a  
destination, wherein the header register is  
configured to store header information corresponding  
to the one of the frames, and wherein the transmit  
logic is coupled to the transmit buffer and the  
header register and is configured to read the header  
information in the header register and to transmit  
the one of the frames from the transmit buffer to  
the destination based on the header information.